# Voltage Amplifier Design Report

ELEC 305 - Spring 2024

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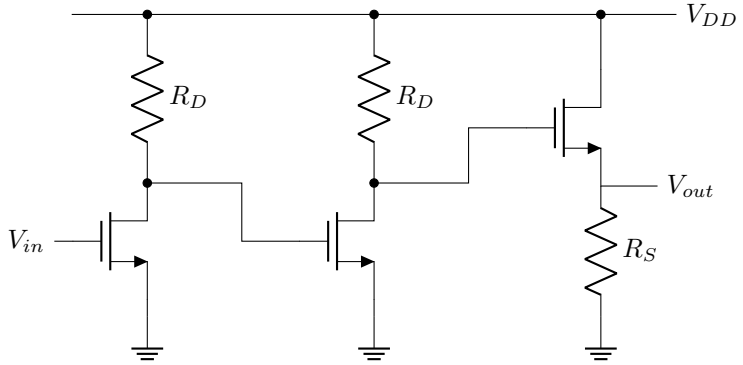
**Matthew Nutt**

## Design Theory

This project centers around the design of a MOSFET voltage amplifier following specific requirements. The required attributes of the MOSFET voltage amplifier are as follows:

| | |
|---|---|
| $V_{DD}$ | $\leq 1.5\,\text{V}$ |
| Frequency | $1\,\text{kHz}$ |
| Total DC Current | $\leq 2\,\text{mA}$ |
| Magnitude of Voltage Gain | $\geq 20\,\text{dB}$ |
| Input Impedance | $\geq 100\,\text{k}\Omega$ |
| Output Impedance | $\leq 30\,\Omega$ |
| Reference Current of Current Mirrors | $10\,\mu\text{A}$ |

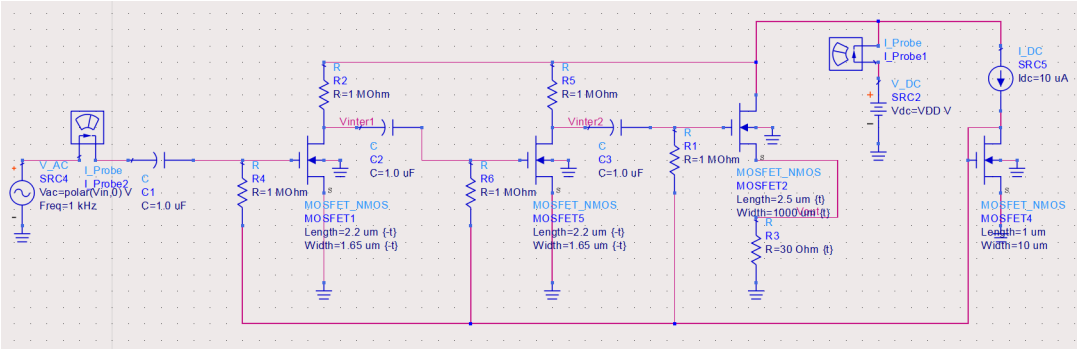
Based on these requirements, a three-stage amplifier is an appropriate solution. Specifically, two common-source (CS) stages followed by a final common-drain (CD) stage. The output CD stage provides low output impedance, but suffers from excessive attenuation. This signal loss is balanced by the high gain of the CS stages, which also provide high input impedance.




The above schematic shows the design of the amplifier circuit, without the biasing network. The value for $R_D$ is $1\,\text{M}\Omega$, the maximum allowable resistance, as the output impedance of the intermediate stages is irrelevant, whereas a high gain is necessary to offset the CD stage. The value for $R_S$ is $30\,\Omega$, as output impedance $\leq 30\,\Omega$ is required, and with the parallel resistance of the MOSFET, the output impedance is guaranteed to meet the specification.

# Final Design

The Keysight ADS schematic below shows the final design of the amplifier. Changes include the addition of a MOSFET biasing network and current probes for verifying performance (more details in Simulated Performance).

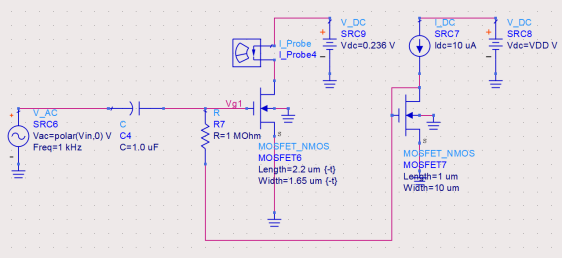


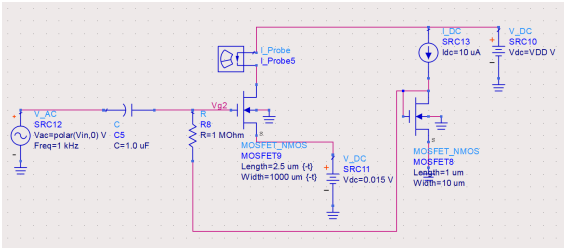

Although values for the resistors in the amplifiers were predetermined, values for the other passive components had to be chosen upon integration of the biasing network. The capacitance of 1 $\mu$F and the resistance of 1 M$\Omega$ were selected for the capacitors and resistors, respectively, as those were the maximum allowable values: The goal was to minimize the cutoff frequency of the highpass filter formed by the biasing network, in order to minimize signal attenuation.

The sizes of the MOSFETs were determined experimentally. By utilizing the Keysight ADS tuning tool, optimal values for width and length could be quickly located, although the width of the third MOSFET was limited by practical constraints. After tuning, the first two MOSFETs were given a length of 2.2 $\mu$m and a width of 1.65 $\mu$m. The third MOSFET had a length of 2.5 $\mu$m and a width of 1000 $\mu$m. Additionally, all MOSFETs used 10 parallel fingers, effectively multiplying their width $\times 10$.

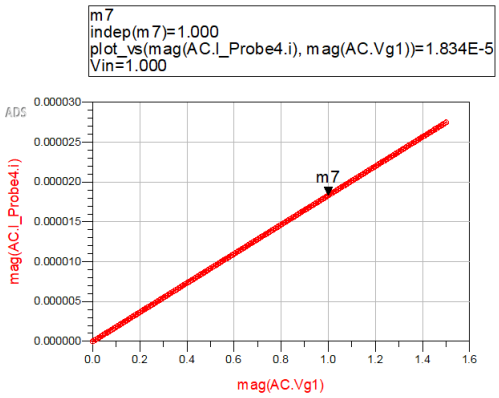
# Theoretical Performance

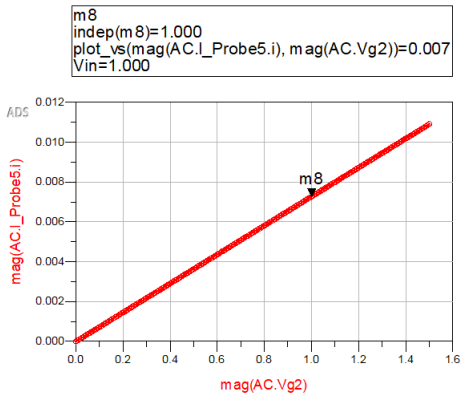
In order to determine the transconductance $g_m$ for the two different MOSFET configurations, testing circuits were made as shown:




The input signal and biasing network were left unchanged, but the resistor at the drain/source was replaced with a constant DC voltage source, as fluctuations in the biasing conditions due to the voltage drop of the resistor would interfere with measurements of transconductance. The voltages of the sources were determined by a DC analysis of the original circuit in operating condition. The results of these tests are shown below:




From this testing setup, the transconductance of the first two MOSFETs was determined to be $g_m = 18.3\,\mu\text{S}$. The value for the third MOSFET was $g_m = 7\,\text{mS}$.

With these measurements, the theoretical performance of the amplifier can be determined:

The gain of the amplifier is the product of each stage's gain. The gain of the first two CS stages is $|A_v| = g_m R_D = (18.3 \times 10^{-6})(10^6) = 18.3$, or $25.2\,\text{dB}$. The gain of the final CD stage is $|A_v| = \frac{R_S g_m}{1+R_S g_m} = \frac{(30)(7\times10^{-3})}{1+(30)(7\times10^{-3})} = 0.174$, or $-15.2\,\text{dB}$. Therefore, the overall gain is $|A_v| = 58.1$, or $35.3\,\text{dB}$.

The input impedance of the amplifier is determined by the input impedance of the first stage. As the first stage is a CS amplifier, the input impedance is theoretically $\infty$.

The output impedance of the amplifier is determined by the output impedance of the final stage. As the final stage is a CD amplifier, the output impedance is $R_{\text{out}} = \frac{1}{g_m} \parallel R_S = \frac{1}{(7\times10^{-3})} \parallel (30) = 24.8\,\Omega$.

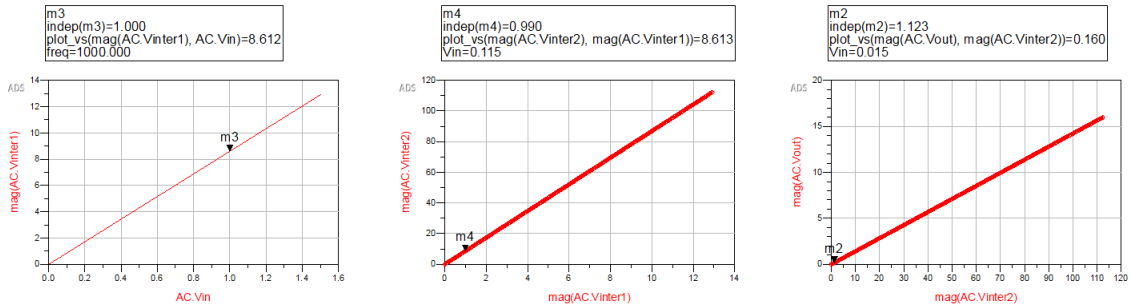
| Parameter | Theoretical |
|---|---|
| Magnitude of Voltage Gain | 35.8 dB |
| Input Impedance | $\infty$ |
| Output Impedance | $24.8\,\Omega$ |

# Simulated Performance

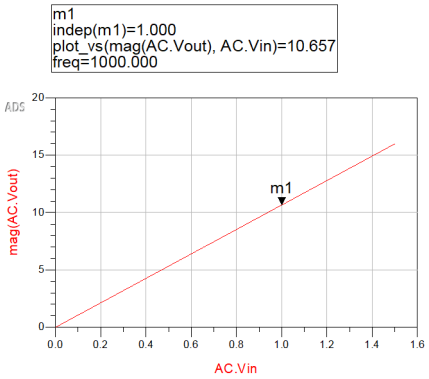
In order to determine the simulated attributes of the amplifier, various testing arrangements were made, as described in the sections that follow.

## Gain

The original amplifier circuit is arranged to measure the gain of each stage and of the entire amplifier by comparing input voltages to output voltages. The gain for the CS stages was measured to be 8.61 in the simulation, and the CD stage had a gain of ∼0.15, as shown by the plots below:

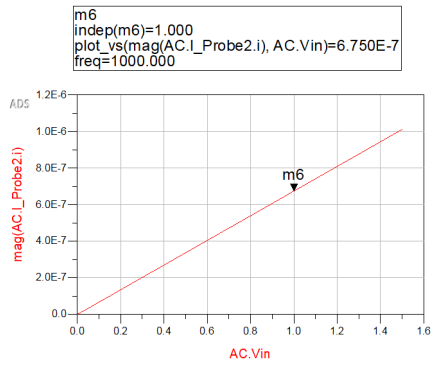



The voltage gain of the entire amplifier was likewise measured in the simulation, with a gain of 10.65, or 20.55 dB:



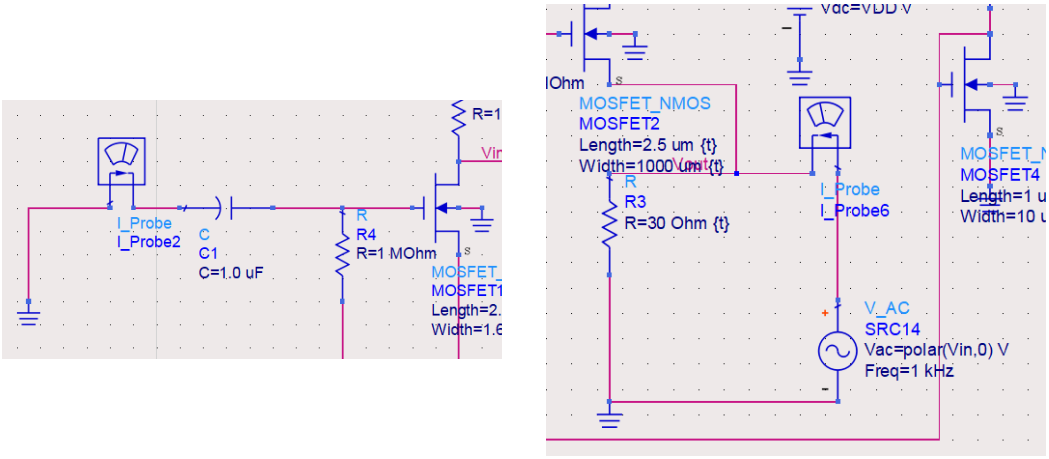

## Input Impedance

Similarly to the gain, the input impedance can be measured in the original amplifier configuration, in this case by comparing the input AC voltage to the AC current recorded by a current probe. The plot below is inverted (i.e., measures current vs voltage instead of voltage vs current, as the latter resulted in incomprehensible results from Keysight ADS), so the input impedance was simulated to be 1.48 MΩ.

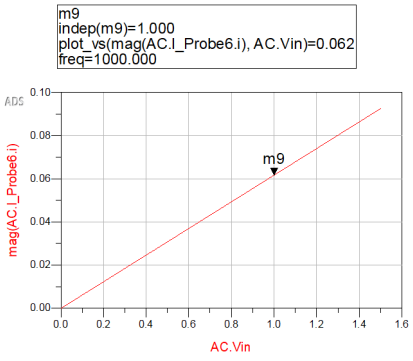



## Output Impedance

Measuring the output impedance of the amplifier required changes to the voltage amplifier. Namely, the voltage source generating $V_{in}$ was replaced by ground, and a voltage source was added to the output of the amplifier, in conjunction with a current probe. These changes are pictured below:

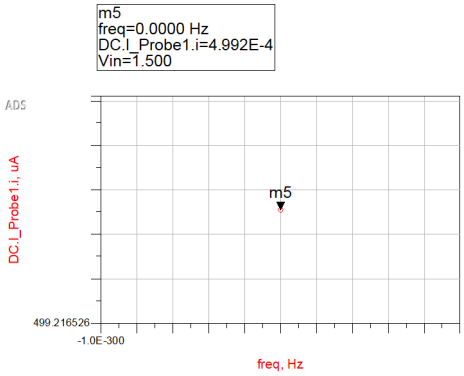



With these changes, the relationship between the test voltage and measured current was simulated to generate the plot below. Again, the axes are inverted due to the limitations of Keysight ADS, so the output impedance was measured to be 16.1 Ω.



### Miscellaneous

The total DC current was measured in the original amplifier, with a current probe. The resulting current was simulated to be 0.5 mA:




The other specifications are also met by the amplifier: $V_{DD}$ was set to be 1.5 V, simulations were performed at a $V_{in}$ frequency of 1 kHz, and a single current source of 10 $\mu$A was used as a reference for the biasing network.

## Summary

Summarizing the results of the project, a comparison table of theoretical and simulated results is shown below:

| Parameter | Theoretical | Simulated | Requirement |
|---|---|---|---|
| Magnitude of Voltage Gain | 35.8 dB | 20.55 dB | $\geq$ 20 dB |
| Input Impedance | $\infty$ | 1.48 M$\Omega$ | $\geq$ 100 k$\Omega$ |
| Output Impedance | 24.8 $\Omega$ | 16.1 $\Omega$ | $\leq$ 30 $\Omega$ |

It is evident that there are major discrepancies between the calculated/theoretical results, and the simulated results given by Keysight ADS. The reduction in gain for all three stages can be explained by Channel Length Modulation (CLM), as the effective output resistance $r_0$ of the MOSFETs reduces the gain of each amplifier. The non-infinite input impedance is likely due to gate leakage; the gate of a MOSFET forms a capacitor with the substrate, and just like capacitors, electrons can (rarely) cross the oxide separating their parallel plates. Finally, the lower output impedance can also be explained by CLM, as the effective resistor $r_0$ provides another path for current to flow through the circuit. Assembling and simulating the circuit was critical for designing an amplifier that compensates for these effects, along with others not mentioned, as theory will only take you so far.